Chapter 6

Field Effect Transistors

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Electronics: Principles, Concepts and Practices

Table of contents

Intro

What is FET?

1. FET is an acronyms for Field Effect Transistors.
2. It is a fundamental building block of modern electronic devices and circuits.
3. It is a three-terminal, voltage controlled, device and is categorized as shown in Fig. 1.

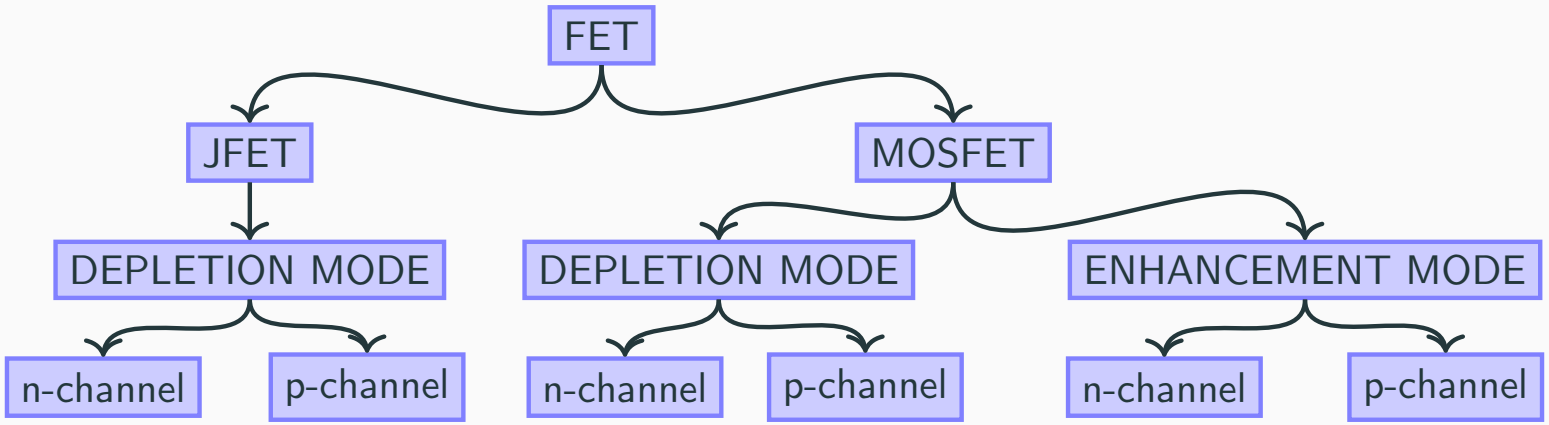


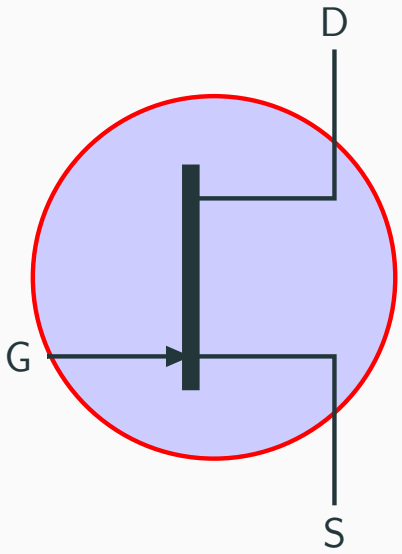
Figure 1: Classification of FET

JFET

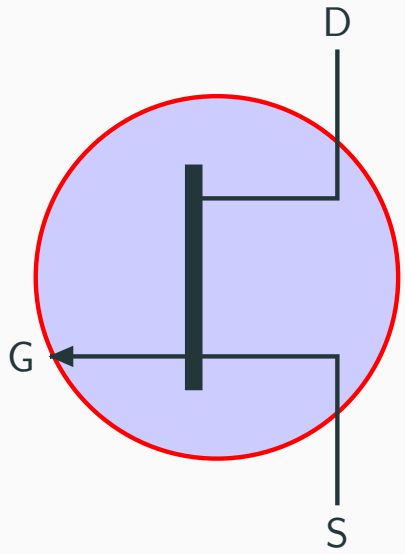
JFET

JFET is a three-terminal device that conducts current through either electrons or holes, depending on whether it is an n-channel or a p-channel JFET respectively.

The circuit symbols for the n-channel and p-channel JFETs are shown in Figure 2.



(a) n-channel circuit symbol



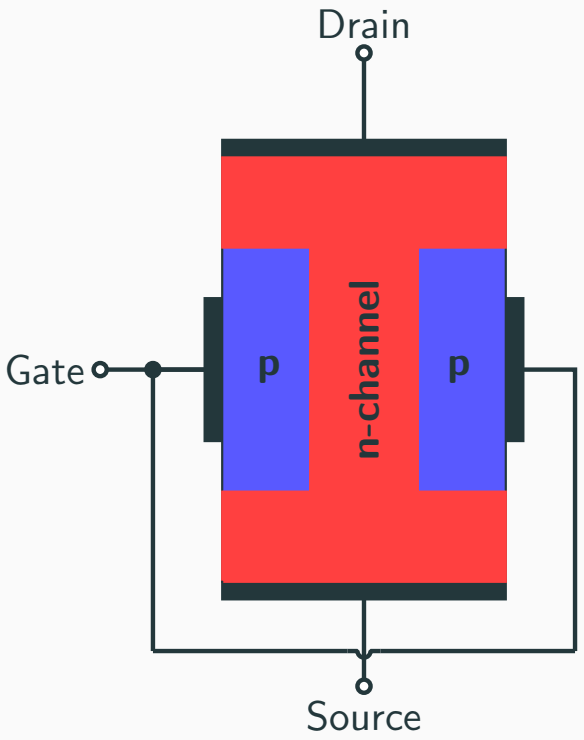
(b) p-channel circuit symbol

Figure 2: Circuit symbol of JFET

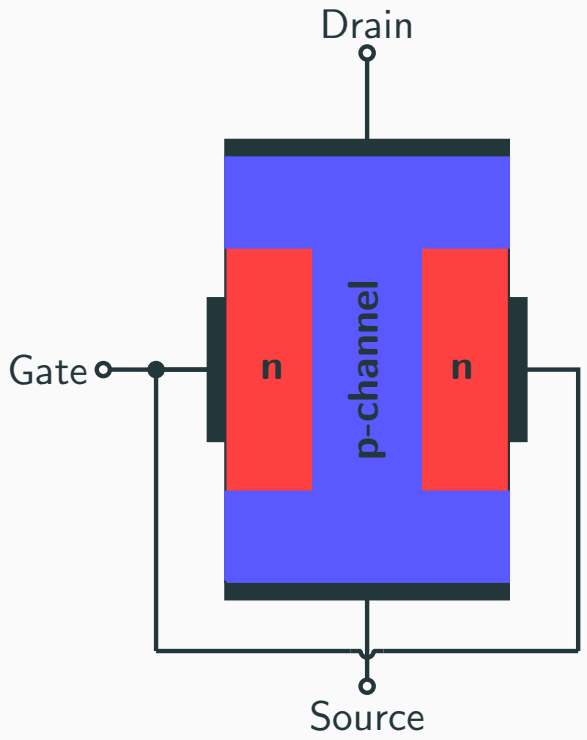
JFET Construction

Figure 3 is the longitudinal cross sections of the n-type and p-type JFETs.

They consist of a lightly doped p-type or n-type silicon bar, known as the channel, encircled by a heavily doped substrate of the opposite charge.



(a) n-channel JFET

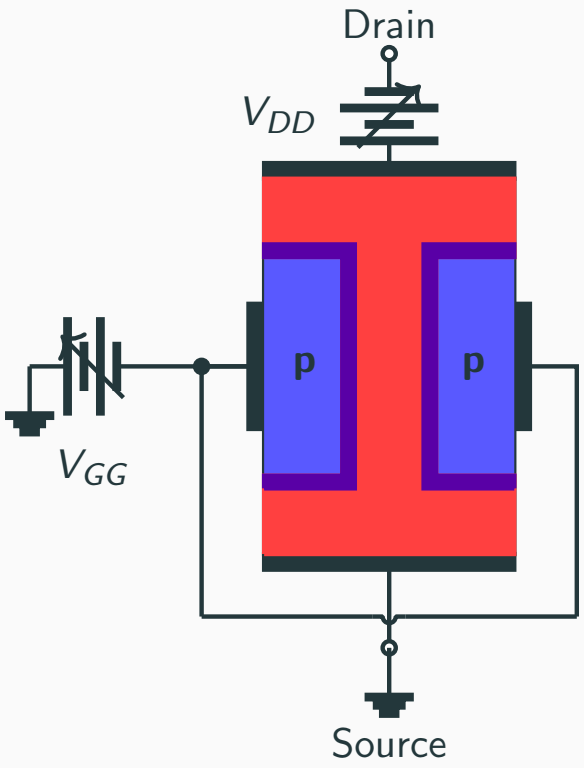


(b) p-channel JFET

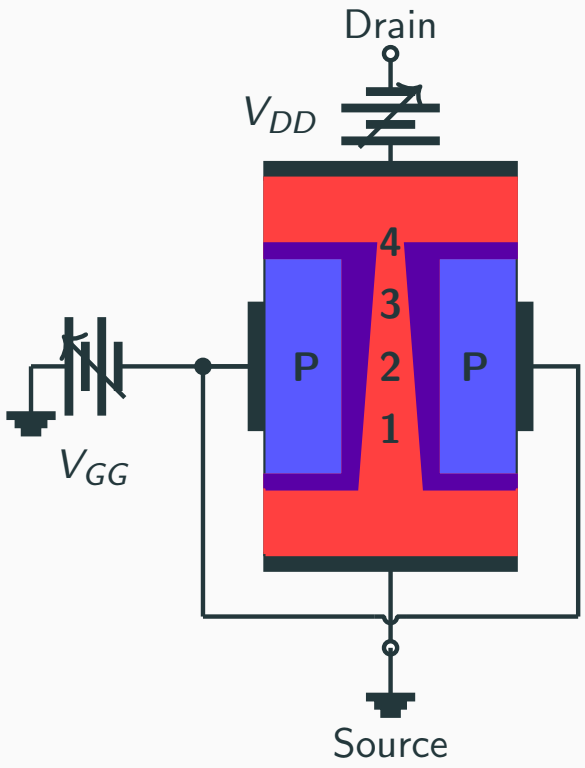
Figure 3: JFET construction

JFET Operation

Fig. 5 and Fig. 4 illustrate the operation of the JFET under various biasing conditions as indicated.



(a) $V_G = 0$ V and $V_{DD} = 0$ V

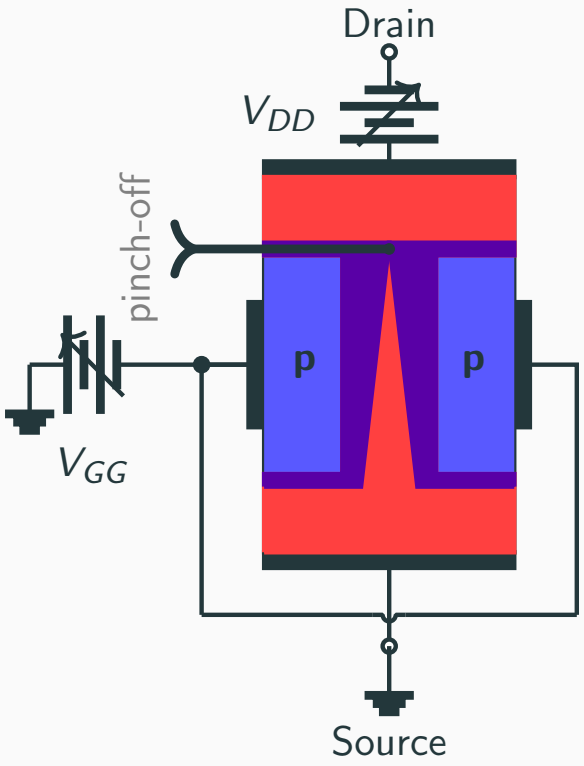


(b) $V_G = 0$ V and $V_{DD} > 0$ V

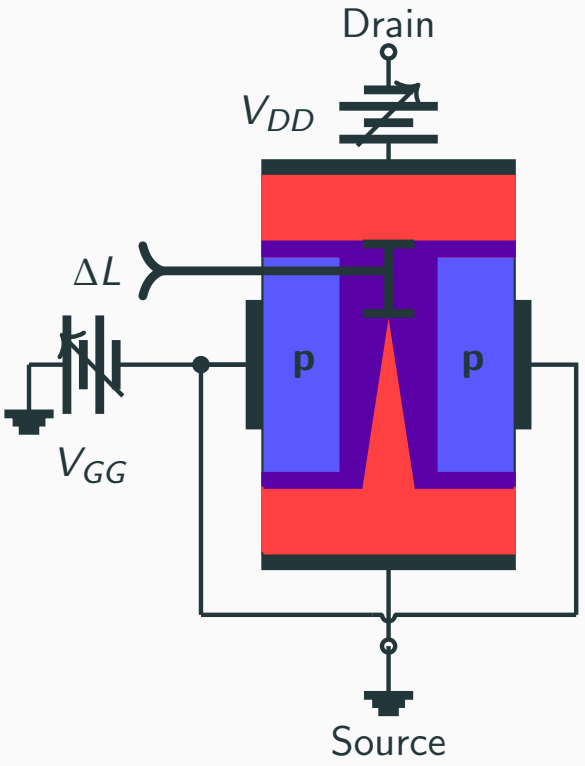
Figure 4: A depiction of JFET operation 1

Pinch-off

As we increase the source-drain voltage V_{DS}, we reach a point where the channel near the drain region practically disappears. This phenomenon is known as pinch-off.



(a) $V_{GG} = 0$ V and $V_{DD} = V_{Dsat}$



(b) $V_{GG} = 0$ V and post pitch-off at $V_{DD} > V_{Dsat}$

The effect of increasing the source-drain voltage beyond pitch-off is reflected in the output characteristic curve shown in Figure 6.

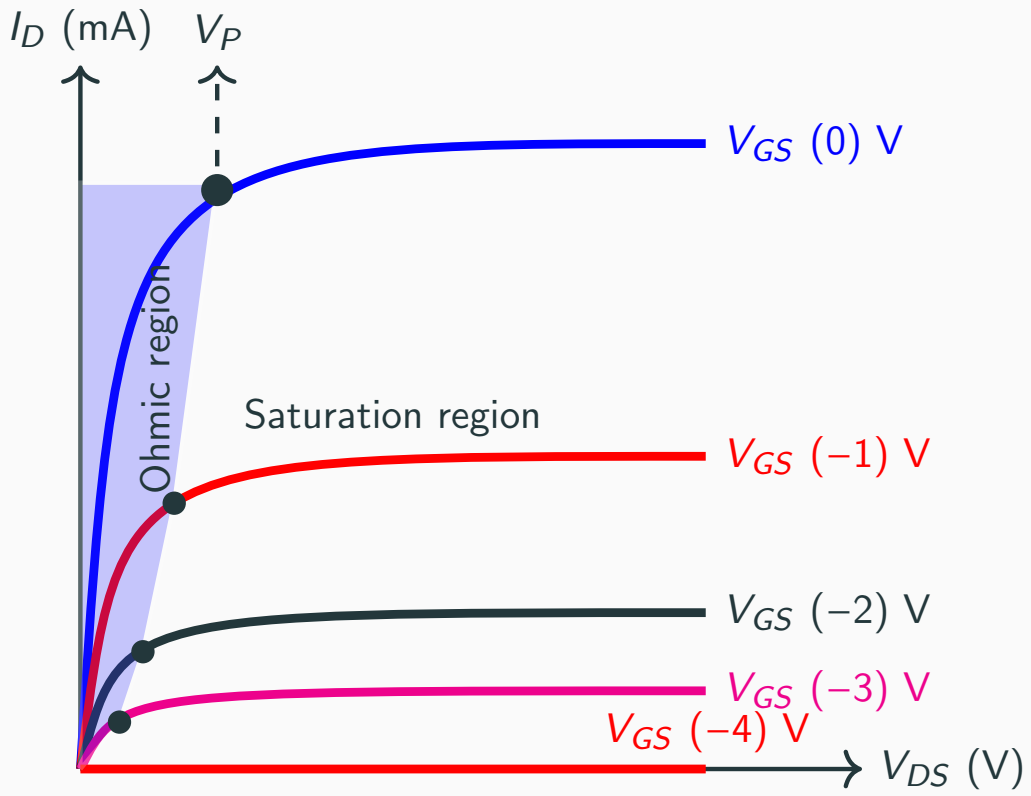


Figure 6: The output characteristics of JFET

Transfer Characteristics

Transfer characteristics relate the output variable as a function of the input variable in relationship to some constants.

For the BJTs, the transfer equation related the output current I_C to the input current I_B when β is constant as shown in Equation (1)

$$I_C = f(I_B) = \beta I_B \tag{1}$$

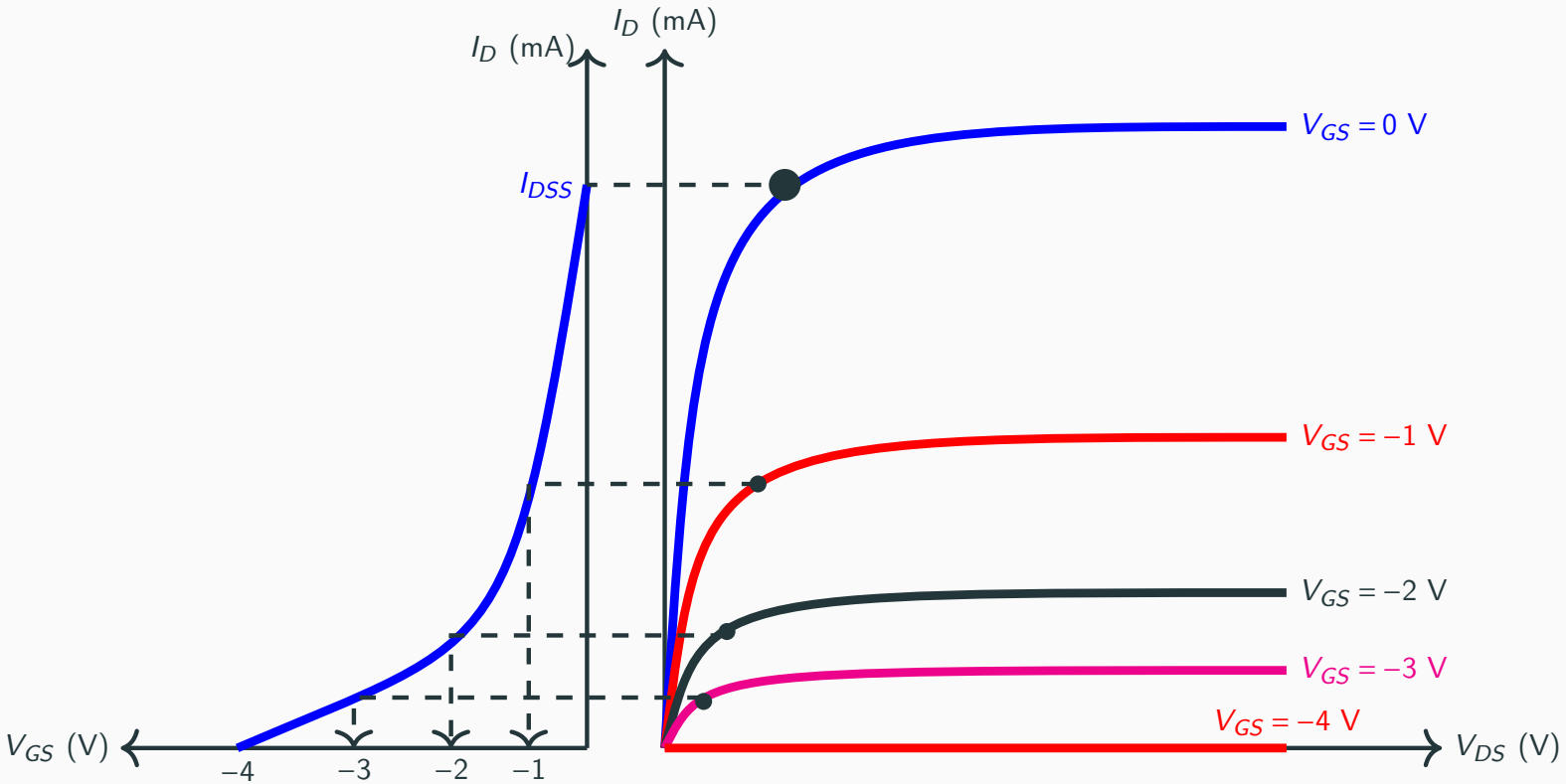
For the FET, The transfer equation is the Shockley equation

$$I_D = f(V_{GS}) = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{2}$$

The transfer curve, illustrated in Figure 7(a), can be derived from Equation (2) or obtained directly from the output characteristic plot shown in Figure 7(b).

It is important to note the following:

1. The maximum drain current, I_D, is defined as I_{DSS} and occurs when $V_{GS} = 0$; and
2. For gate-to-source voltages $V_{GS} = V_P$, the drain current $I_D = 0$ irrespective of V_D.



(a) Transfer characteristic curve

(b) Output characteristic curve

Figure 7: Derivation of transfer characteristics

Operating Region

1. **Ohmic Region:** JFET acts as a voltage controlled resistor. The JFET will be in this region for $V_{DS} < V_P$.
2. **Cutoff Region:** When the gate voltage V_{GS} is below the pitch-off voltage causing the JFET to act as an open circuit.
3. **Active or Saturation region:** We operate the JFET as an amplifier in the region defined for $V_{DS} > V_P$.

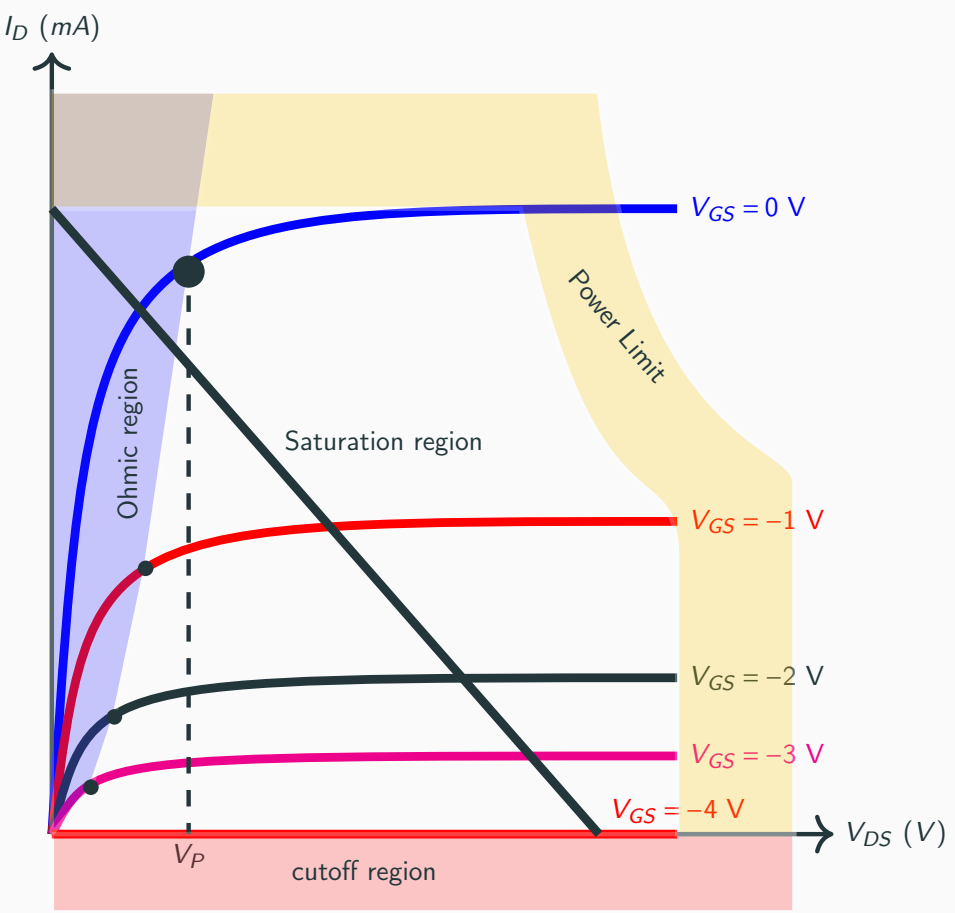


Figure 8: The output characteristics of FET

JFET Configuration

The JFET has three configurations and the choice of configuration depends on the system's specific requirements (such as gain, impedance matching and signal integrity).

The configurations are

1. Common Source Configuration:
   This configuration provides high input impedance, good amplification. Used in amplifiers and signal processing circuits.
2. Common Gate Configuration:
   This configuration has low input impedance, high output impedance. Used in impedance matching circuits and in RF amplifiers.
3. Common Drain Configuration:
   Also known as a source follower. This configuration has high input impedance and low output impedance. It provides a voltage gain close to unity. Used in buffer amplifiers.

JFET Biasing

JFET Biasing

JFETs, like BJTs, require proper biasing when used as amplifiers.

The DC operating points are determined by simultaneously solving the device equation (Shockley equation) and the biasing network equation.

The important device equations for DC analysis of JFETs are:

$$I_G \approx 0A \tag{3}$$

$$I_D = I_S \tag{4}$$

$$I_D = f(V_{GS}) = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{5}$$

Next, we develop network equations from the biasing network.

The solution to the combined device and network equations determines the current and voltage levels associated with the operating point.

There are several biasing network configurations, but in this text, we will discuss:

1. Fixed-bias configuration,
2. Self-bias configuration and
3. Voltage-divider biasing.

Fixed-bias configuration

By applying KVL to this circuit, we can derive the following equations:

$$V_{GS_Q} = -V_{GG} \tag{6}$$

Equation (6) may now be substituted into the Shockley device Equation (5) to obtain

$$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GG}}{V_P}\right)^2 \tag{7}$$

Applying KVL to the output loop to obtain

$$V_{DS_Q} = V_{DD} - I_{D_Q} R_D \tag{8}$$

The resulting equivalent DC circuit for fixed-bias circuit is depicted in Fig. 9.

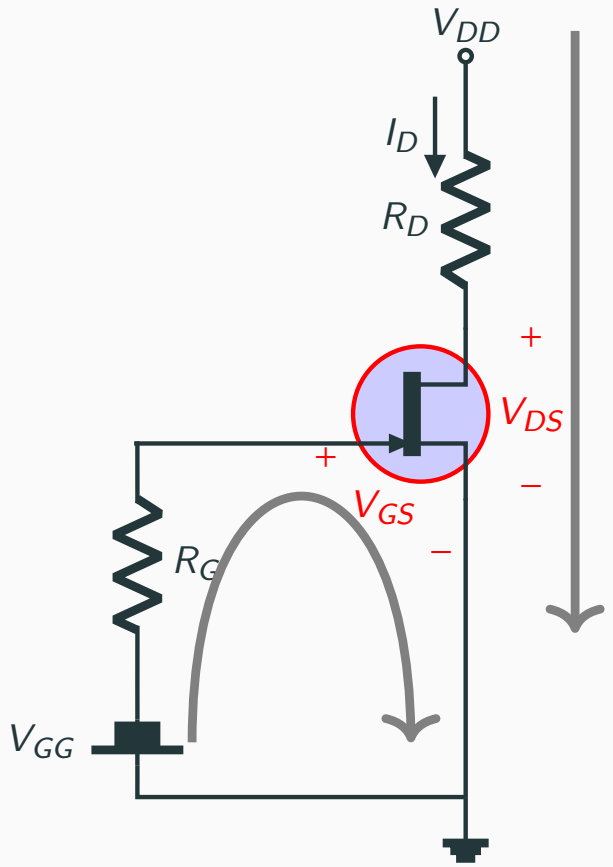


Figure 9: Fixed-bias network

Fixed-bias configuration

A graphical approach can also be obtained by finding the point of interception between the transfer Equation (5) and the network Equation (6) as shown in Fig. 10.

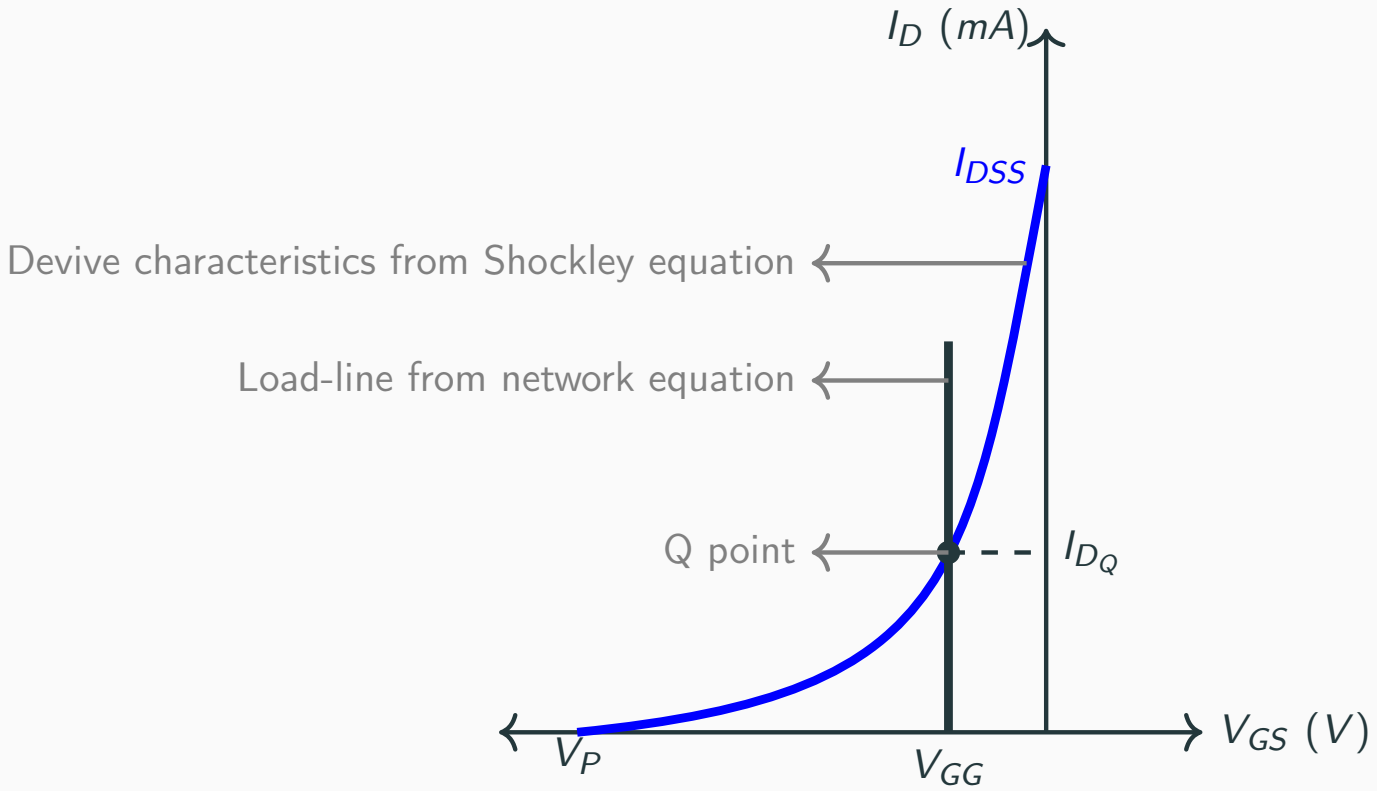


Figure 10: Graphical solution for fixed-bias network

Self-bias configuration

The network equations:

$$V_{GS_Q} = -I_D R_S \tag{9}$$

Substituting into the Shockley device Equation (5) to obtain

$$I_{D_Q} = I_{DSS}\left(1 - \frac{I_D R_S}{V_P}\right)^2 \tag{10}$$

Applying KVL to the output loop to obtain

$$V_{DS_Q} = V_{DD} - I_{D_Q}(R_S + R_D) \tag{11}$$

The self-bias circuit is depicted in Fig. 10.

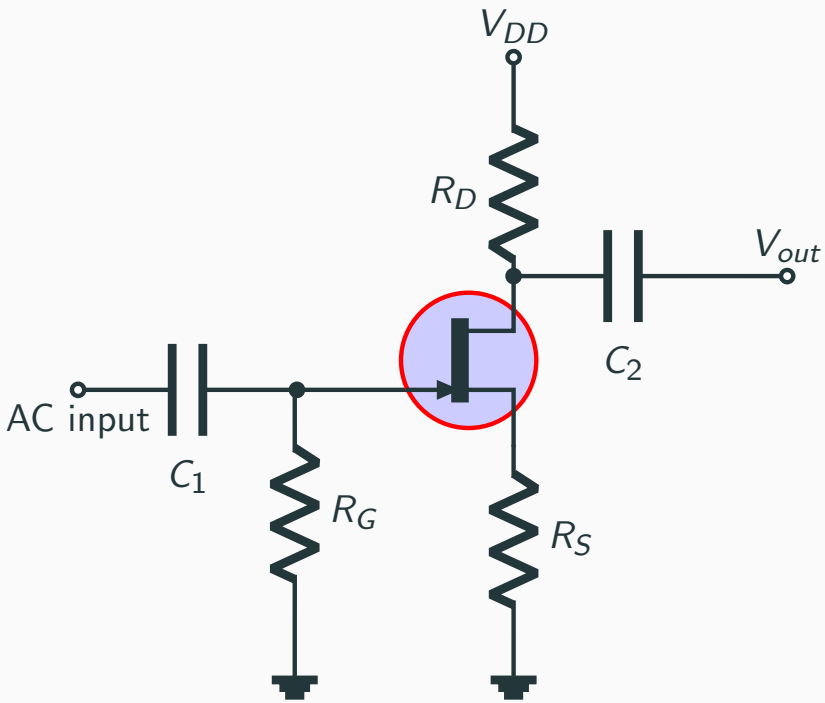


Figure 11: self-bias network

Self-bias configuration

A graphical solution obtained by finding the point of interception between the plots of the transfer Equation (5) and the network Equation (9) is shown in Fig. 11.

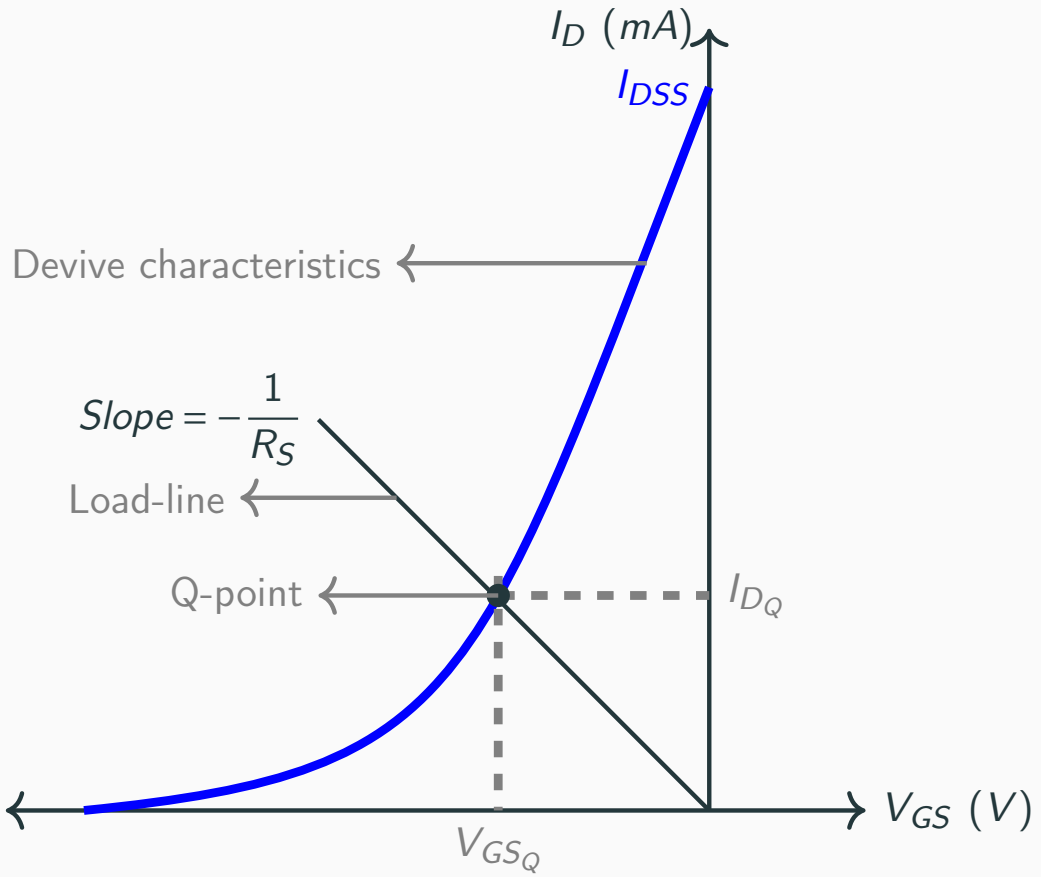


Figure 12: Graphical solution for self-bias network

Voltage-divider biasing

The DC equivalent circuit of a voltage divider biasing circuit is depicted in Fig. 13.
The network equation:

$$V_{GS_Q} = V_G - I_D R_S \qquad (12)$$

Solving Equation (12) and Equation (5) to obtain the Q-point. Applying KVL to the output loop to obtain

$$V_{DS_Q} = V_{DD} - I_{D_Q}(R_S + R_D) \qquad (13)$$

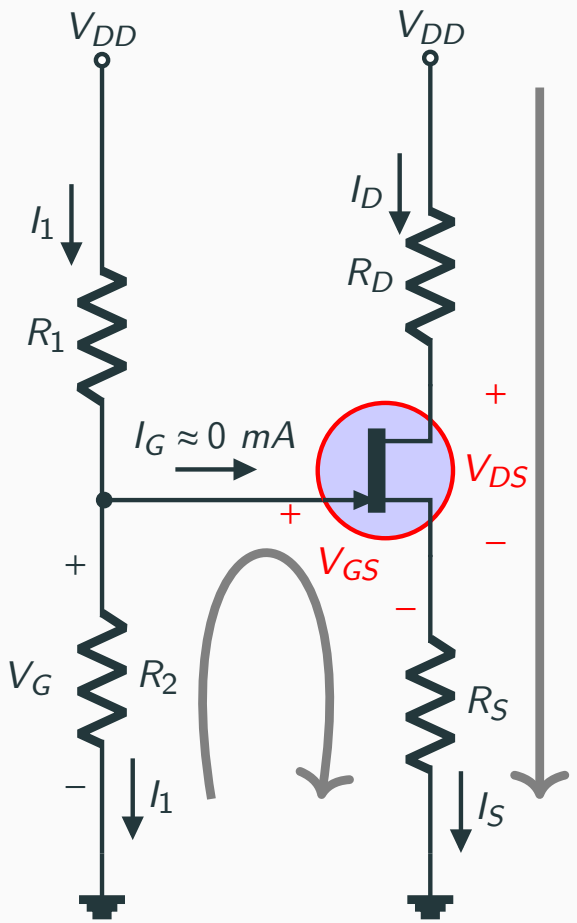


Figure 13: Voltage-divider bias configuration

MOSFET

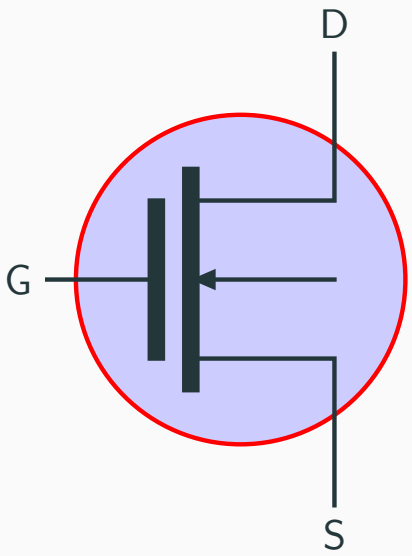
MOSFET

- The field-effect transistor (FET) can be broadly classified into two categories: JFET and MOSFET.
- MOSFET stands for Metal-Oxide-Semiconductor Field-Effect Transistor.
- The term "metal oxide" refers to the gate material, which is typically made of aluminum and is insulated from the channel by a thin layer of silicon dioxide (SiO_2).
- MOSFET can be further divided into two types: Depletion-type MOSFET (DMOSFET) and Enhancement-type MOSFET (EMOSFET).
- Unlike DMOSFET, EMOSFET has unique device characteristics and equations that differ from the Shockley's equation, which was previously applied to JFET and is also applicable to DMOSFET.

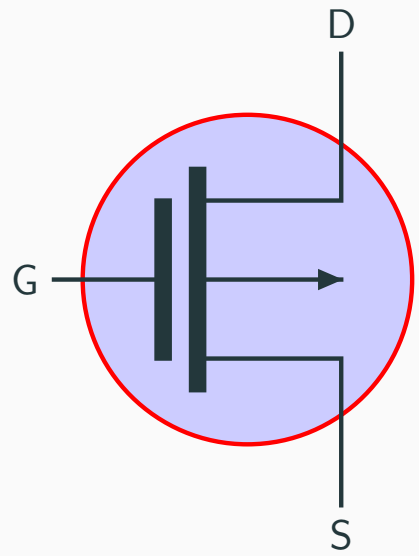
DMOSFET

The DMOSFET could be either an n-channel or p-channel depletion-type MOSFET.

The circuit symbols for the n-channel and p-channel DMOSFETs are provided in Figure 14.



(a) n-channel circuit symbol

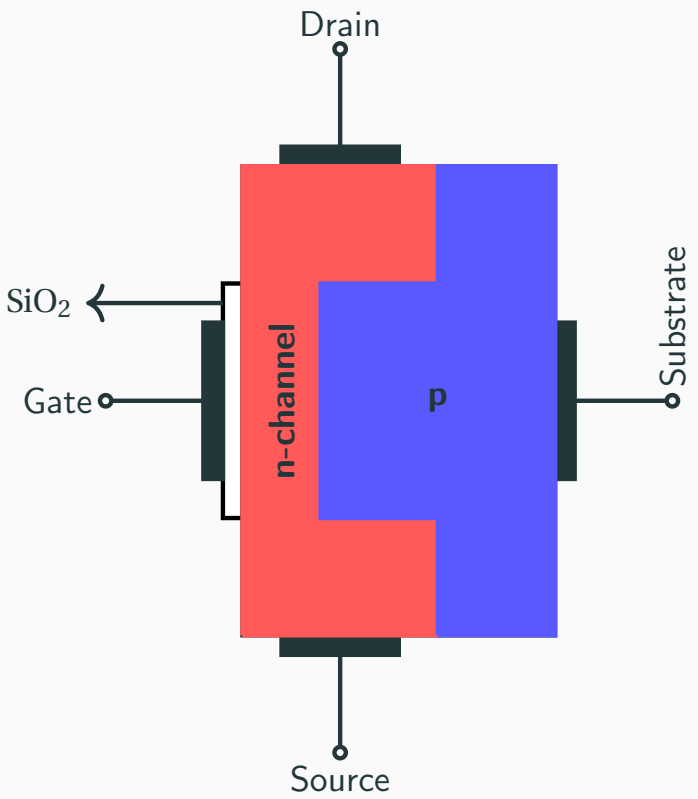


(b) p-channel circuit symbol

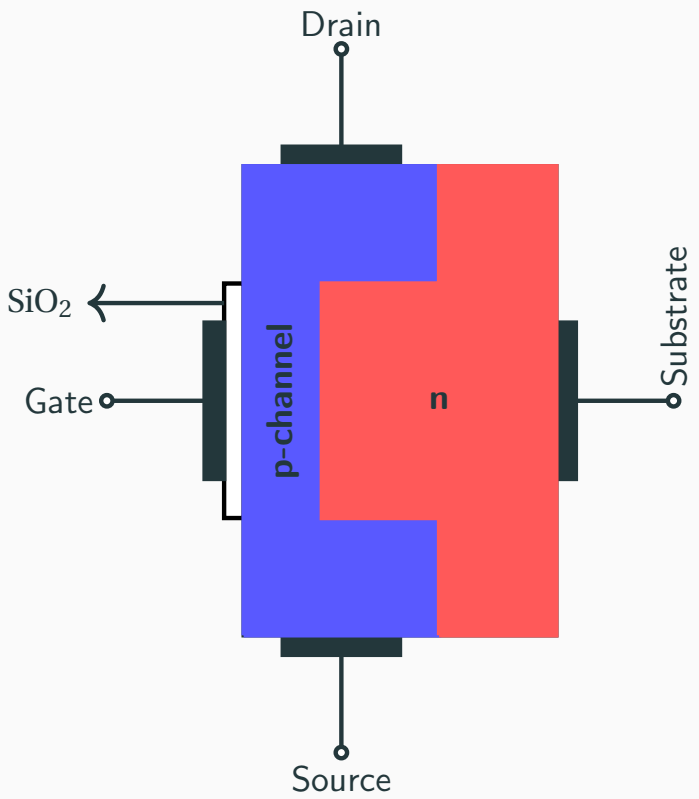
Figure 14: Circuit symbol of MOSFET

DMOSFET Construction

The Gate is connected to a metal contact surface, but it remains insulated from the n-channel by a thin layer of silicon dioxide.



(a) n-channel DMOSFET



(b) p-channel DMOSFET

Figure 15: Depletion-type MOSFET construction

References i